UM10177

8 A PoL converter using SOT23 MOSFETs

Rev. 02 — 21 December 2007 **User manual**

Document information

Info	Content
Keywords	SOT23 MOSFET PoL PMV45EN demo board
Abstract	Point of Load (PoL) converters are at the leading edge of power supply performance in terms of power density and efficiency, however, performance is not everything and the $/W value is also critical. This demo board returns benchmark efficiency and power density using industry standard construction and operating conditions to get 8 A output using NXP PMV45EN SOT23 MOSFETs. The user manual describes the key features of the design to enable customers to achieve the performance benefits in their designs. A scalable approach has been applied to allow alternative MOSFET packages to be used for higher powers.

Revision history

Rev	Date	Description
01.00	20060302	First issue
02.00	20071221	Second issue

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1. Introduction

The SOT23 demo board demonstrates the performance of NXP SOT23 MOSFETs in an operational single-phase buck converter on a small 2.5 cm × 5.0 cm board. The board is supplied with three MOSFETs with locations for adding an additional FET. When implemented with the recommended current limit circuits, these parts deliver surprising power loads.

The simple, low cost board is designed for operation from an input voltage of 12 V nominal, but is capable of operation from 5 V to 13 V. As supplied, the board output voltage, V_{OUT}, is set to 1.2 V. V_{OUT} can be adjusted from 0.8 V to 5 V by changing a single resistor. The current limit resistor should also be altered with changes in output voltage. The SOT23 devices (see Figure 1) used on this board are NXP PMV45EN. The MOSFETs are rated at 5.4 A maximum.

For detailed specifications, refer to the respective MOSFET data sheets. The use of a pair of these MOSFETs allows the board to provide continuous output currents up to 5 A max with adequate airflow. As supplied, this board can achieve an 8 A output current with three MOSFETs.

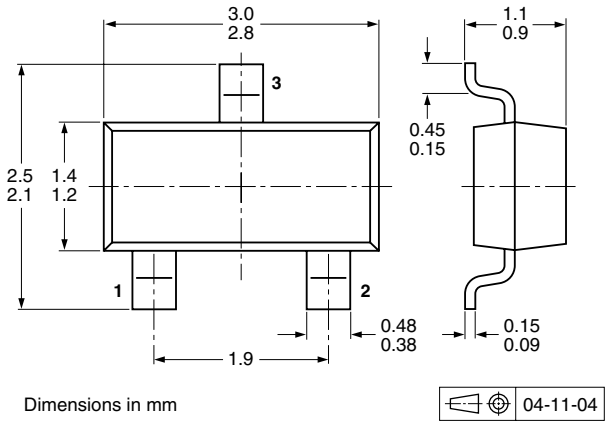

Fig 1. Simplified outline

Figure 1 shows the FET footprint. The demo board uses large pads for the drain and source to provide heat sinking. The MOSFET outline plus clearance will occupy less than 200 mm × 200 mm.

The TI TPS40071 controller was selected for its feature set which includes: voltage operating range of 4.5 V to 28 V, high side current limit, source and sink drivers, and anti-cross conduction protection. For controller technical information, see the TI data sheet for the TPS40071.

The board was designed as a simple low cost 8 A small form factor PoL demonstrator. For V_{OUT} values above 2.5 V, add a fourth FET. For ease of evaluation, the design area was not minimized.

1.1 Board top and bottom views

Figure 2 shows the top and bottom view of the board. All components are located on the topside and clearance between components is expanded so attaching meters and probes is less difficult. Power input connections, power output connections, and mounting hole pads are mirrored top and bottom.

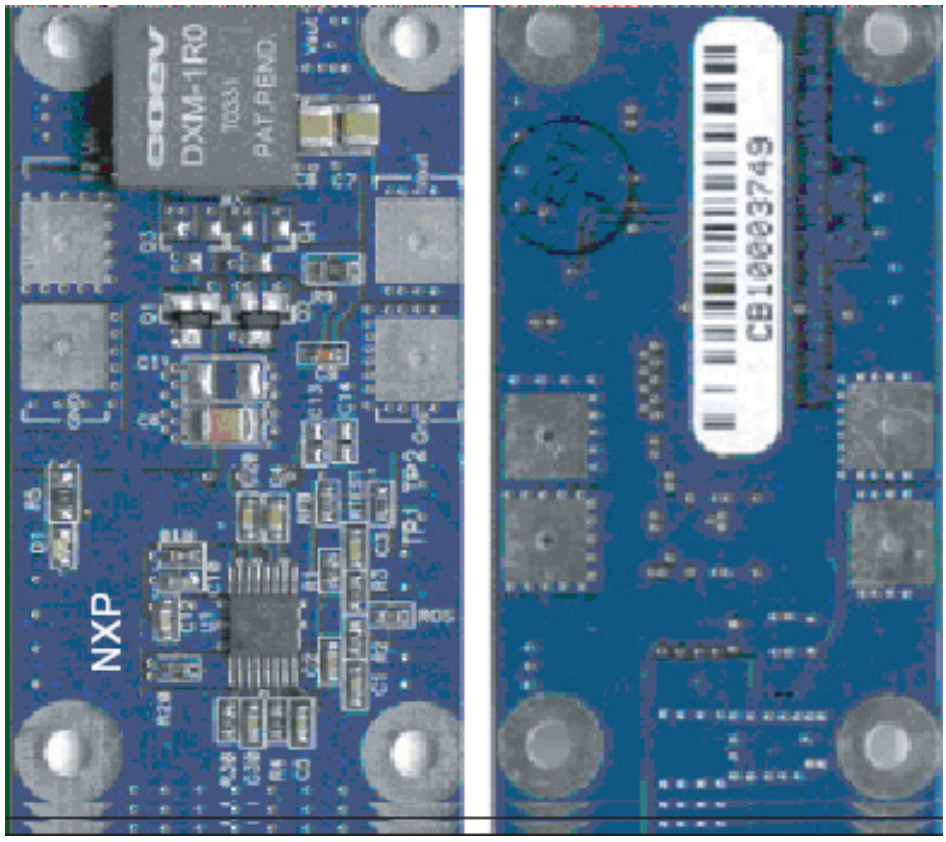

Fig 2. Board top and bottom views

1.2 Connection details

Figure 3 shows the board connections. Input power and ground connection pads are at the top of the board, and output power and ground connection pads at the bottom. The pads are large and mirrored on the board top and bottom side for current handling capability. You can use solder connections or alligator clips to make the power attachment.

Soldering to the connections pads will reduce the voltage drop of the connection. Small holes in the input and output pads are sized so conductive posts can be inserted for oscilloscope and meter probes. Mounting holes in the corners of the board are connected to power ground.

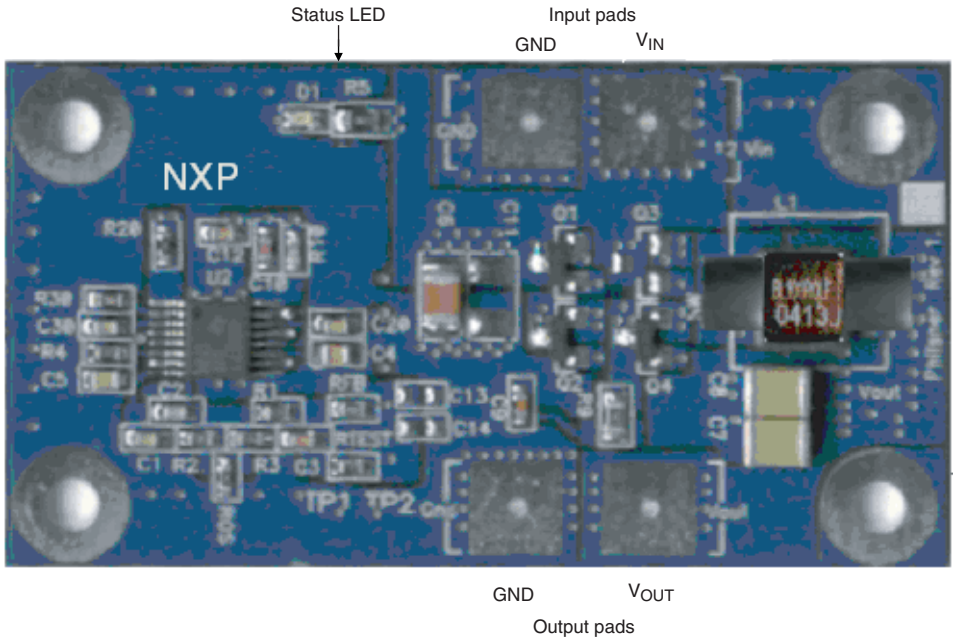

Fig 3. Input - output pads

2. Design criteria

As supplied, the board is designed to provide an output voltage of 1.2 V and 8 A. The output voltage can be changed by replacing the resistor connected to the drain. The current limits are set by R10. The operating frequency is 500 kHz. A blue status LED at the top of the board lights when the controller and board are operational. The LED blinks when the high side FET is current limited.

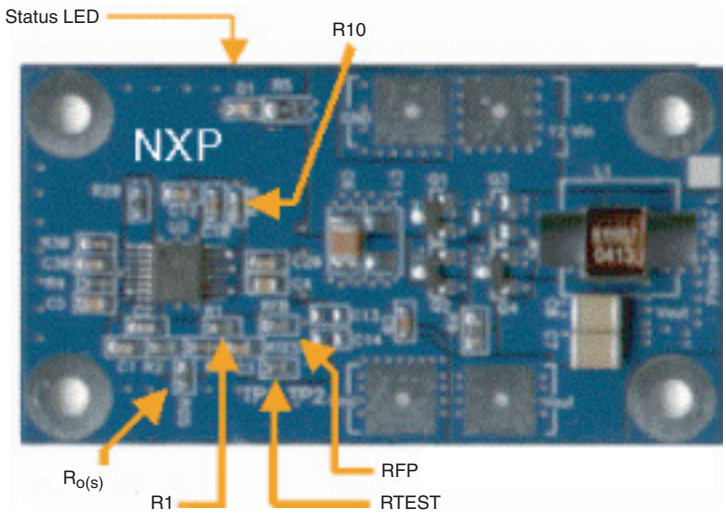

Fig 4. $R_{o(s)}$ versus V_{OUT}

Table 1. Table $R_{o(s)}$ versus V_{OUT}

	V_{IN} = 12 V				
V_{OUT}	$R_{o(s)}$	R10	Number of syncs	FETs control	Max I_O
0.8 V	60.4 kΩ	0.698 kΩ	1	1	4.5 A
0.8 V	60.4 kΩ	1.27 kΩ	2	1	9.0 A
1.2 V	11.7 kΩ	1.58 kΩ	1	1	5.0 A
1.2 V	11.7 kΩ	2.32 kΩ	2	1	8.5 A
1.51 V	7.32 kΩ	3.24 kΩ	2	1	9.0 A
2.5 V	3.32 kΩ	3.16 kΩ	1	1	5.0 A
3.3 V	2.32 kΩ	3.57 kΩ	1	1	5.0 A
3.3 V	2.32 kΩ	4.02 kΩ	2	1	6.1 A
3.3 V	2.32 kΩ	2.55 kΩ	2	2	8.5 A
5.0 V	1.40 kΩ	4.12 kΩ	1	1	5.0 A

2.1 Board features

As mentioned previously, the output voltage can be easily adjusted by changing the value of a single resistor, $R_{o(s)}$. The chart in Figure 4 lists some of the tested configurations. The current limit can be adjusted, as described in Section 2.1.2. R10 will need to be readjusted for a safe current limit when changing the board V_{OUT}. The feedback path has been designed so that phase-gain testing can be performed by removing a single resistor. The following sections describe these features in more detail.

2.1.1 V_{OUT} selection

Replacing $R_{o(s)}$ with the values calculated in the equation below changes V_{OUT}

$$R_{o(s)} = R1 * V_{ref} / (V_{OUT} - V_S)$$

Where V_{ref} is the reference voltage of the operational amplifier, and is fixed at 0.7 V for the TPS40071. Resistor values for common output voltages are provided in Figure 4.

2.1.2 Control FET current limit

The TPS40071 data sheet has equations for calculating R10 for a desired current limit. The TPS40071 compares the voltage drop across R10 with the voltage drop across the control FET R_{DSon} at full conduction and initiates a shut down if the control FET voltage drop exceeds the R10 reference voltage drop.

The blue LED will flicker during cycle-to-cycle shutdown. The FET voltage drop is a function of R_{DSon} and is temperature dependent. The precise shutdown value depends on the FET operating temperature. See the TPS40071 data sheet for additional information on current limit settings.

The R10 shutdown value was selected so the FET case temperature would not exceed 90 °C in an ambient of 25 °C with airflows of 200 LFM. Higher currents are achieved by adding more FETs. You must alter the value of R10 to allow for the increased current.

2.1.3 Increasing output current capability

When the ratio of V_{OUT} to V_{IN} is small, the duty cycle is correspondingly small. The control FET power loss is multiplied by the duty cycle D, and the sync FET is multiplied by (1-D). For low output voltages, most of the power loss is in the sync FET. For lower voltages, output current capability is significantly increased by adding an additional sync FET.

As V_{OUT} increases, the power loss is shared more equally between the sync and control FETs. For higher V_{OUT} ranges, you must add an additional control and sync FET for increased current capability.

2.1.4 Phase gain testing

Phase gain testing (Bode plots) can be performed by removing the zero ohm RFP resistor and injecting a test signal across RTEST, a 50 W resistor as shown in Figure 5. By monitoring the response at TP2 to the injected signal at TP1, you can generate a phase gain plot by varying the frequency of the test signal.

The full details of this test are beyond the scope of this manual, but the measurements are easily done using a Vector Network Analyzer (VNA). Please refer to the TPS40071 data sheet for loop compensation techniques. The zero ohm RFP resistor should remain in the circuit for normal operation.

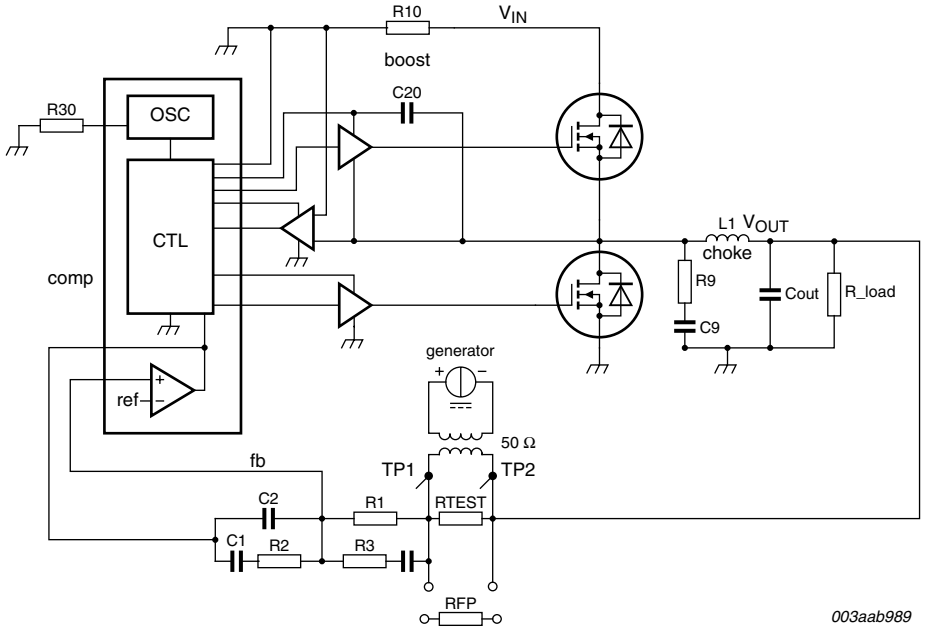

Fig 5. Phase gain test setup

2.2 Board schematic

The board schematic is shown in Figure 6 (current limit shown for two FETs).

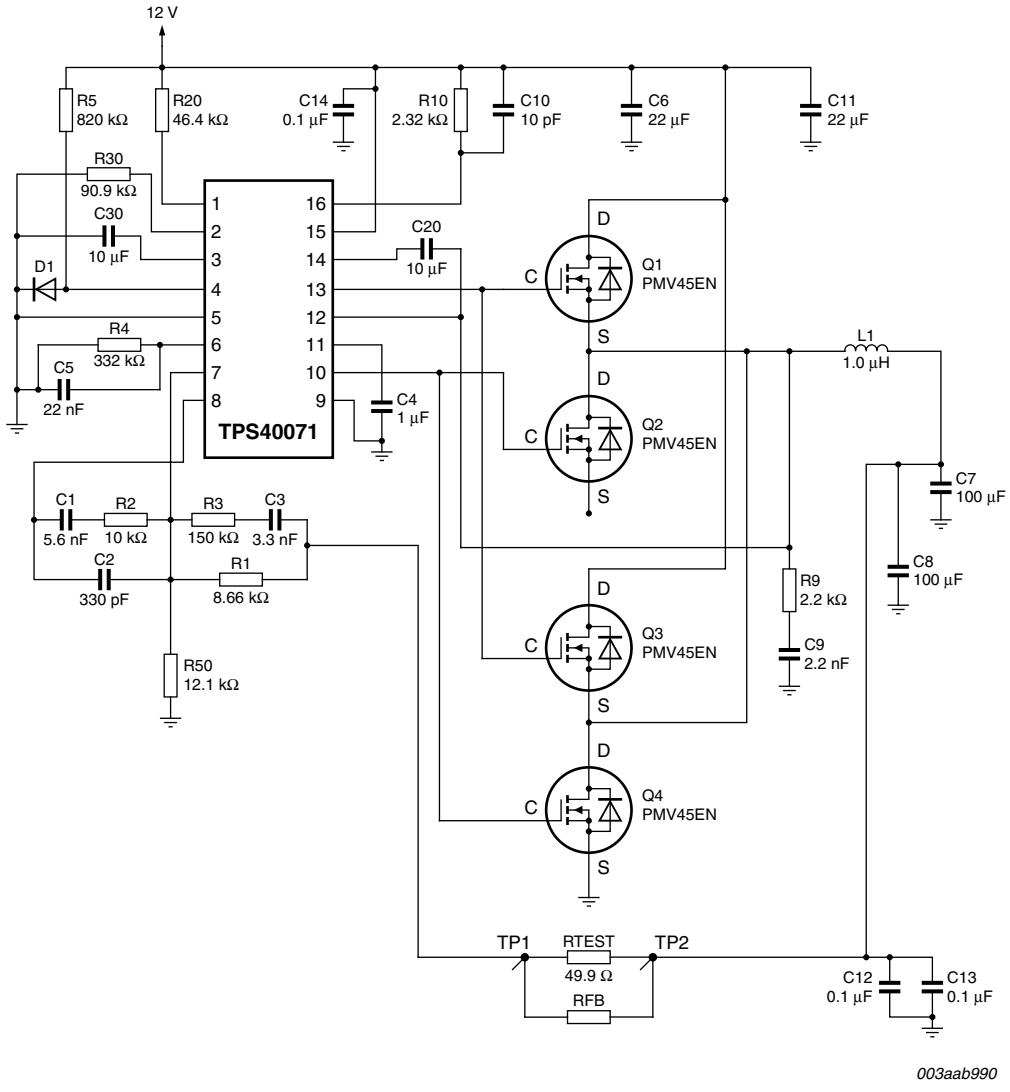

Fig 6. Board schematic

2.3 Layout

The demo board is a four-layer board, all 1 oz. copper. All signals are routed top and bottom with the inner layers dedicated to power and ground with one exception, the gate signals are wide traces in the inner layers (see Figure 7). The board was designed to minimize high current induced noise in the input drive and controller circuit areas. The input current flows in a tight loop between the input pads, the input decoupling caps and the MOSFETs.

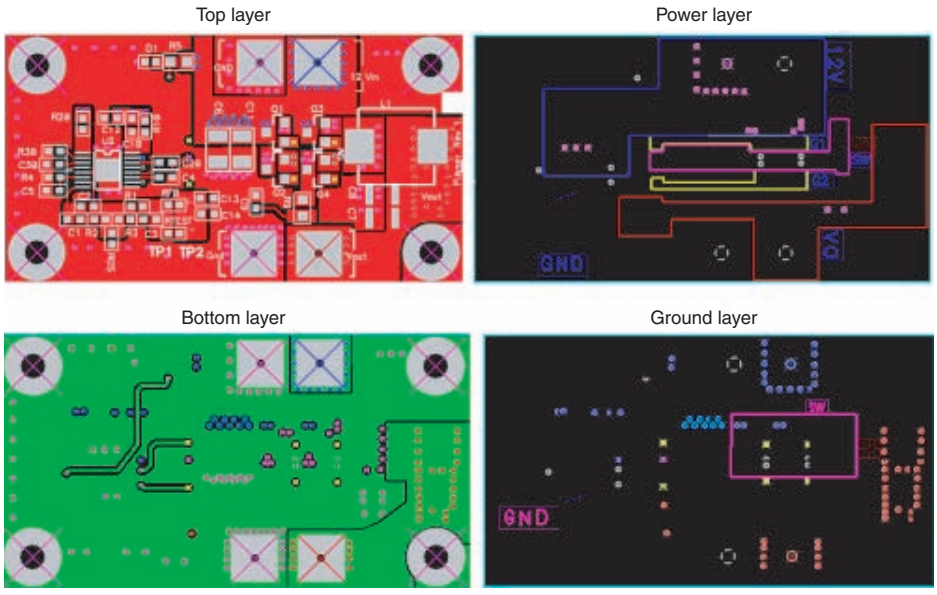

Fig 7. Board layouts

3. Electrical and thermal performance

The demo board, with two FETS, is capable of 5 A output currents for V_{OUT} values ranging from 1.2 V to 5 V. Three FETS raises this to 8 A. Below 1.2 V, I_{out} drops to 4.5 A. This rating is based on a 90 °C case temperature limit, a 25 °C ambient temperature, and airflow of 200 LFM.

3.1 Efficiency sweeps

Efficiency is plotted in Figure 8 for V_{OUT} voltages of 1.2 V and 3.3 V. The input voltage is 12 V for both sweeps. The maximum current swept is the level that produces 90 °C FET case temperatures. Higher currents can be achieved with greater airflow.

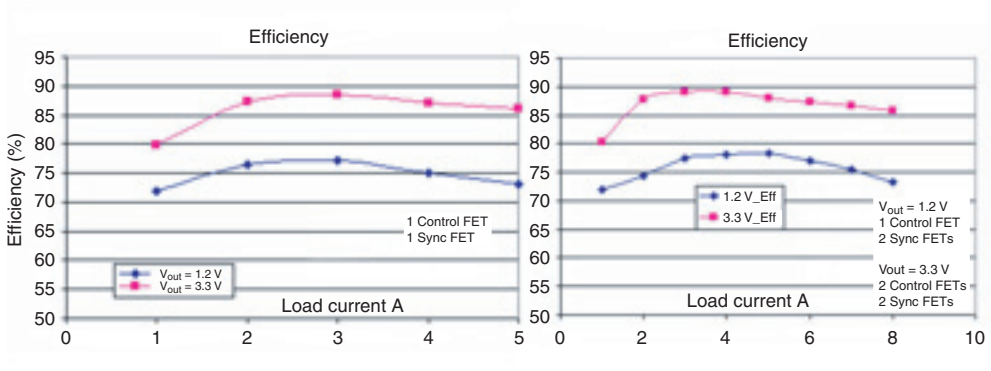

Fig 8. Efficiency sweep for 1.2 V and 3.3 V output voltages

3.2 Thermal sweeps

Figure 9 shows the thermal case temperature of the control and sync FETs for the efficiency sweeps in Figure 8. The load current is swept from zero amps to a maximum level which is defined when the average of the two case temperatures equals 90 °C.

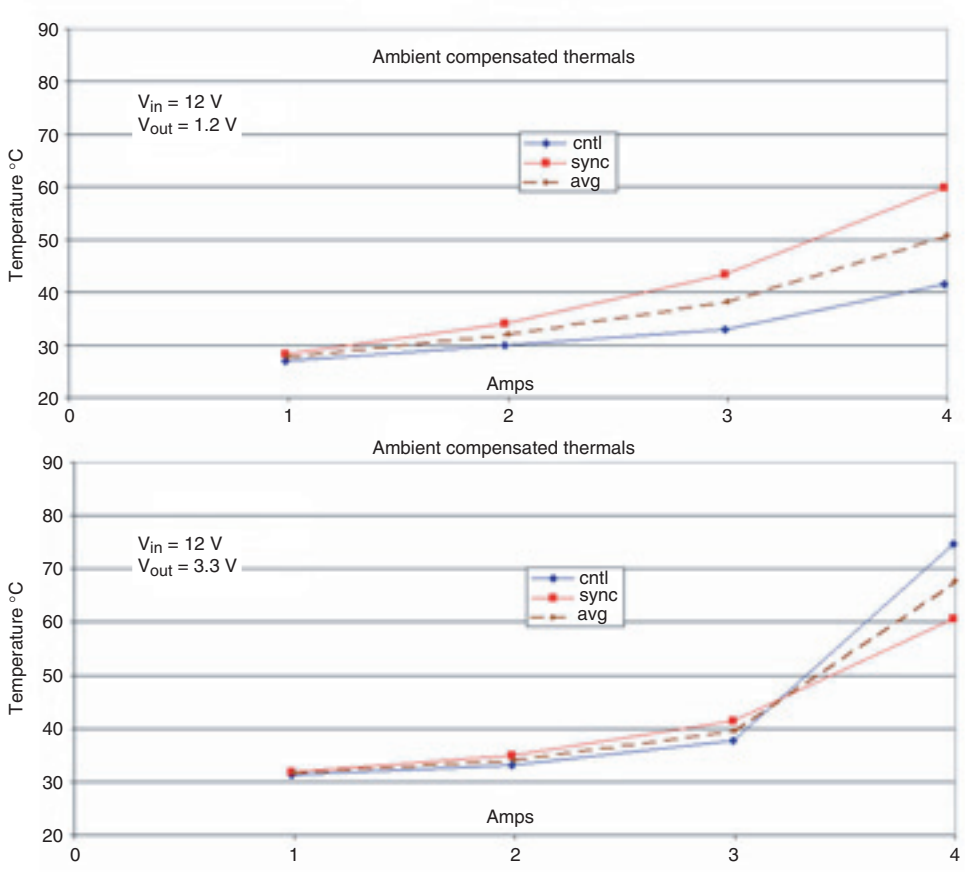

Fig 9. Thermal measurement

3.3 Electrical waveforms

The scope shots in Figure 10 and Figure 11 show the sync FET gate, control FET gate, switch node, and boost voltage simultaneously for a no load and a 5 A load respectively.

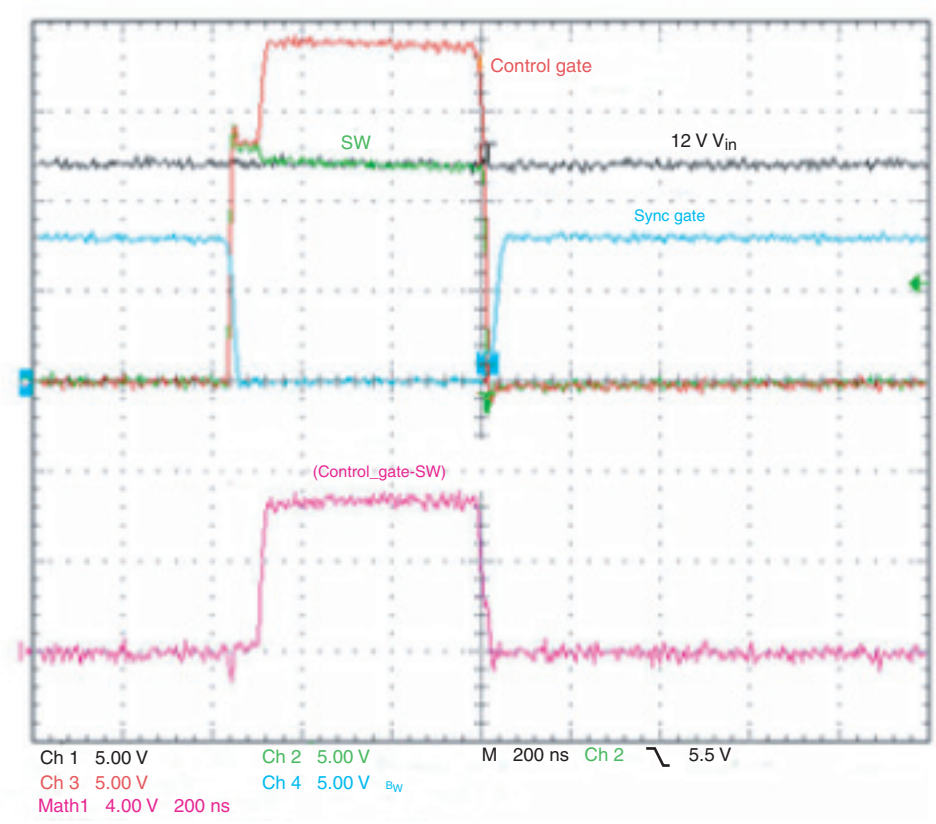

Fig 10. Waveforms no load

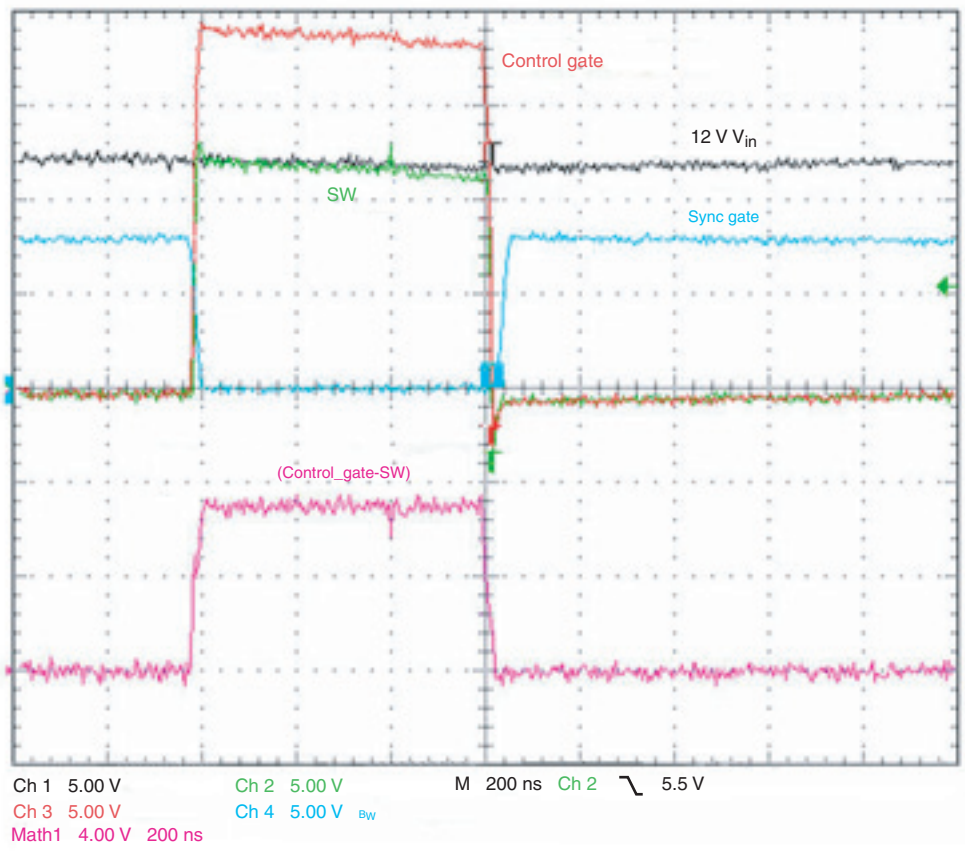

Fig 11. Waveforms at 5 A

3.4 Loop gain phase plot

Figure 12 shows the loop gain and phase versus frequency for V_{OUT} = 3.3 V. The compensation was very nearly the same for V_{OUT} ranges of 0.8 V to 3.3 V. The test setup is shown in Figure 6.

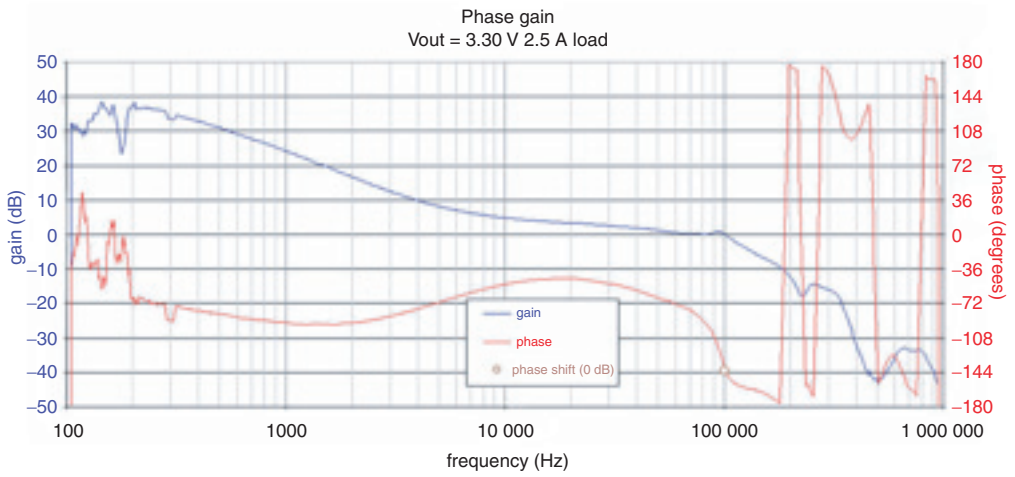

Fig 12. Phase gain plot of demo board

4. Bill of materials

Table 2. Pilsner rev 1.0 - 1-phase

Item	Qnt	Value	Package	Tolerance	Rating	Manufacturer	Manufacturer P/N	Designation
1	1	3.3 nF	603	± 10 %	50 V	TDK	-	C 3
2	1	10 pF	603	± 10 %	50 V	TDK	-	C 10
3	1	220 pF	603	± 10 %	50 V	TDK	-	C 2
4	1	2.2 nF	603	± 10 %	50 V	TDK	-	C 9
5	1	22 nF	603	± 10 %	50 V	TDK	-	C 5
6	1	5.6 nF	603	± 10 %	50 V	TDK	-	C 1
7	3	0.1 μF	603	± 10 %	50 V	TDK	-	C 12, C 20, C 30, (C 13, C 14 empty)
8	1	1 μF	603	± 10 %	16 V	TDK	-	C 4
9	1	22 μF	1210	+ 80 %, – 20 %	16 V	TDK	-	C 6 (C 11 empty)
10	2	100 μF	1812	+ 80 %, – 20 %	6.3 V	TDK	-	C 7, C 8
11	1	90.0 k	603	± 1 %	-	-	-	R 30
12	1	8.66 k	603	± 1 %	-	-	-	R 1
13	1	332 k	603	± 1 %	-	-	-	R 4
14	1	2.49 k	603	± 1 %	-	-	-	R 10
15	1	10 k	603	± 1 %	-	-	-	R 2
16	1	12.1 k	603	± 1 %	-	-	-	ROS
17	1	46.4 k	603	± 1 %	-	-	-	R 20
18	1	150	603	± 1 %	-	-	-	R 3
19	1	49.9	603	± 1 %	-	-	-	RTEST
20	1	2.2	603	± 5 %	-	-	-	R 9

Table 2. Pilsner rev 1.0 - 1-phase

Item	Qnt	Value	Package	Tolerance	Rating	Manufacturer	Manufacturer P/N	Designation
21	1	820	603	± 5 %	-	-	-	R 5
22	1	1	603	± 1 %	-	-	-	RFB
23	1	TPS40071	SOP	-	-	TI	TPS40071PWP	U 1
24	1	PMV45EN	SOT23	-	-	NXP	PMV45EN	Q 1, Q2 (Q3. Q4 empty)
25	1	Blue LED	603	-	3.8 V	Lite-On	LTST-C190UBKT	D 1
26	1	HM73-101R0	-	± 20 %	1 μH, 8.5 A	BI	HM73-101R0	L 1

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Date of release: 21 December 2007
Document identifier: UM10177_2